Claims 1, 2 and 4 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,681,770 issued to Ogura *et al.* ("Ogura").

Ogura does not disclose the invention recited in claim 1. Claim 1 recites a structure that includes an oxide layer and an oxide test region "of the same material as said oxide layer and having the same thickness and the same electrical characteristics as said oxide layer." Ogura does not disclose an oxide test region having any of the above-quoted features. The Examiner points to the layers 115 and 117 of Figure 4G of Ogura as being the oxide layer and oxide test region, respectively, but those layers are not of the same material and do not have the same thickness or the same electrical characteristics. The layer 115 is formed by growing oxide on a silicon substrate 104, and thus, the layer 115 is silicon oxide. In contrast, Ogura reports that the layer 117 is composed of nitrogen and oxygen and is deposited on the poly layer 114. In addition, Ogura never states or implies that the layer 117 has the same thickness as layer 115. In fact, because of the differences in the processes for forming the layers 115, 117 (e.g., growing layer 115 on substrate versus depositing layer 117 on poly layer 114), it would be almost impossible to obtain the same thickness for both layers 115, 117.

In addition, claim 1 further recites that the oxide test region is separated from the oxide layer by a field oxide region. Ogura does not disclose a field oxide region separating the layers 115, 117. Instead, in Ogura the layers 115, 117 are on the same side of the field oxide region 102.

For the foregoing reasons, Ogura does not anticipate claim 1.

Claims 2 and 4 depend on claim 1, and thus, are not anticipated for the reasons expressed above. In addition, amended claims 2 and 4 recite other elements not found in Ogura. Amended claim 2 recites that the structure includes a polycrystalline region having a closed perimeter that completely surrounds a central opening in the polycrystalline region. None of the poly layers of Ogura has such a closed perimeter surrounding a central opening. Claim 4 recites that the structure includes a polycrystalline region that laterally completely surrounds and delimits the oxide test region. As shown in Figure 4G, no polycrystalline layer of Ogura laterally completely surrounds and delimits any oxide region. Accordingly, claims 2 and 4 are further distinguished from Ogura.

Claims 3 and 5-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ogura.

Ogura does not teach or suggest the invention recited in claim 3, which depends on claim 1. As discussed above, Ogura does not teach or suggest an oxide test region "of the same material as said oxide layer and having the same thickness and the same electrical characteristics as said oxide layer."

Ogura also does not teach or suggest the invention recited in claims 5-8. In particular, claim 5 recites a structure that includes a polycrystalline region that completely surrounds an oxide test region (taken from claim 6). Contrary to the Examiner's assertion, the polycrystalline region 114 does not completely surround any portion of the dielectric layer 117. Figure 4G is a cross-sectional view in which portions of the poly layer 114 are positioned laterally of the V-shaped portion of the layer 117, but that is not enough to completely surround even the V-shaped portion. As shown in Figs. 4C-4D, the polysilicon gates 110 (mislabeled as 112 in Fig. 4G) extend in elongated lines and thus the V-shaped portion between the gates 110 would also be elongated. As a result, no portion of the poly layer surrounds the V-shaped portion at the front and back ends, that is, looking into the page and from the back side of the page of Fig. 4G. Accordingly, claims 5-8 are nonobvious in view of Ogura.

Although the language of new claims 9-20 differs from that of claims 1-8, the allowability of claims 9-20 will be apparent in view of the above discussion.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

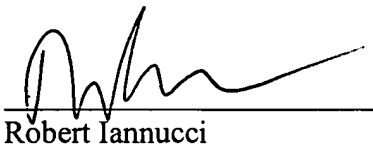
Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made.**"

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Nicola Zatelli et al.

SEED Intellectual Property Law Group PLLC



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 1-2 and 4-7 have been amended as follows:

1. (Amended) A structure for checking an integrated electronic device comprising:

an oxide layer to be measured located above a body of doped semiconductor material and arranged in a position adjacent to a gate region of polycrystalline semiconductor material, said oxide layer having a first area;

an oxide test region of the same material as said oxide layer and having the same thickness and the same electrical characteristics as said oxide layer;

a field oxide region separating the oxide test region from the oxide layer; and

a polycrystalline region of the same material as said gate region, having the same thickness and the same electrical characteristics as said gate region, and positioned adjacent to the oxide test region, said oxide test region having a second area greater than the first area.

2. (Amended) A structure according to claim 1 wherein said polycrystalline region has a closed perimeter that completely surrounds a central opening in the polycrystalline region~~extends along a closed line~~.

4. (Amended) The structure according to claim 1 wherein said polycrystalline region laterally completely surrounds and delimits said oxide test region.

5. (Amended) A structure for checking an integrated electronic device, comprising:

a doped semiconductor material body;

a gate region of polycrystalline semiconductor material;

an oxide layer having a thickness to be determined, located the semiconductor material body, arranged in a position adjacent to the gate region, and having a first area; and

a test region positioned on the semiconductor material body, the test region including an oxide test region of a same material as the oxide layer and having a thickness that is equal to the thickness of the oxide layer, the oxide test region having a second area that is greater than the first area and sufficiently large to be measured in a non-destructive manner by an ellipsometer, wherein the test region further includes a polycrystalline region that completely surrounds the oxide test region.

6. (Amended) The structure of claim 5 wherein the ~~test region further includes a polycrystalline region that completely surrounds~~ oxide layer overlies a first active region of the semiconductor material body and the oxide test region overlies a second active region of the semiconductor material body.

7. (Amended) The test structure of claim ~~6~~ 5 wherein the polycrystalline region has a closed perimeter that completely surrounds a central opening in the polycrystalline region~~extends along a closed line~~.

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